NCV8842PWGEVB

NCV8842 Buck Regulator 7.0 V-16 V to 5.0 V, 3.3 V and 2.5 V @ 1.0 A Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Description

The NCV8842 Evaluation Boards provide a convenient way to implement and evaluate a complete practical buck regulator design. No additional components are required other than the DC input source and load. Separate boards are available for the SOIC−16 and DFN−18 versions of the device. The SOIC−16 board has an input voltage range of 7 V – 16 V and includes jumpers to set the DC output voltage to 2.5 V, 3.3 V or 5.0 V. The DFN−18 board has an input voltage range of 6 V – 16 V and is preset for a nominal output voltage of 3.3 V.

Both boards include SHDNB and SYNC terminals for logic on−off control of the regulator and synchronization of the internal controller to a external frequency source instead of the internal 170 kHz oscillator.

Features

- V^2 Control Method for Uncomplicated Loop Compensation, Fast Transient Response, and Reduced Board Area
- A Total of 12 Components, Including the IC, to Realize a Complete Buck Regulator
- Shutdown Terminal to Disable the Output and Provide a Low Current Drain Standby Mode
- Sync Terminal to Permit Controller Synchronization to an External Source
- 1.5 A Peak Inductor Current
- Cycle−by−Cycle Frequency−Foldback Current Limiter
- Soft Start Function to Reduce Inrush Current
- 87% Efficiency at 1 A Load Current (5 V Output)
- Line Regulation Better Than 0.02%
- Load Regulation Better Than 0.2%

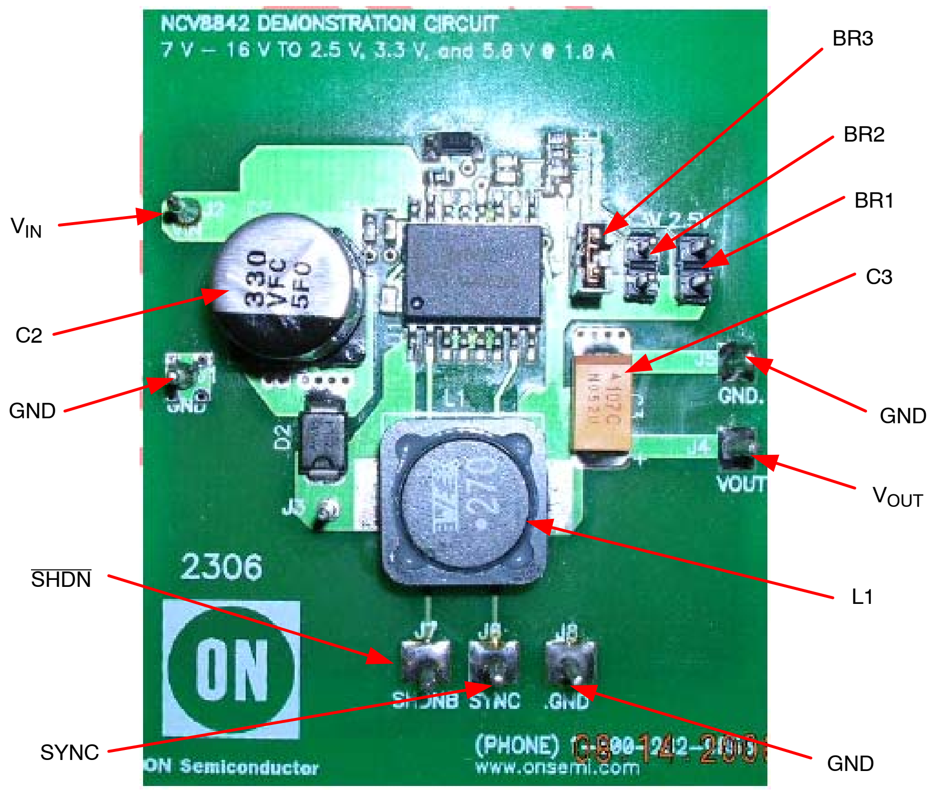


Figure 1. NCV8842 Evaluation Board (SOIC Package)

Table 1. ABSOLUTE MAXIMUM RATINGS

Pin Name	Maximum Voltage	Maximum Current
V_{IN}	16 V	2.0 A
V_{OUT}	10 V	2.0 A
SHDNB	7.0 V	1.0 mA
SYNC	7.0 V	1.0 mA

Stresses exceeding Maximum Ratings may damage the board. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied.

Table 2. NCV8842 SOIC EVALUATION BOARD USER TERMINALS

V_{IN}	Positive DC input voltage, 7 V to 16 V
GND	Common power negative / signal return
V_{OUT}	Regulated DC output voltage
SHDNB	Shutdown−bar signal. Leave open or drive high for normal operation, drive low to force the regulator into sleep/shutdown mode.
SYNC	Input signal to synchronize to converter oscillator to a higher external frequency source. Leave open if unused.
BR1, BR2, BR3	Bridges (jumpers) for programming the regulated output voltage to one of three levels. Always bridge one pair of terminals. Terminals bridged — V_{OUT} BR1 — 2.5 V BR2 — 3.3 V BR3 — 5.0 V

Table 3. ELECTRICAL CHARACTERISTICS
(T_A = 25°C, 7.0 V ≤ V_{IN} ≤ 16 V, 0.1 A ≤ I_{OUT} ≤ 1.0 A, unless otherwise specified.)

Characteristic	Test Conditions	Typ	Unit
Output Voltage			
Voltage Accuracy	–	4.0	%
Line Regulation	No Load	0.02	%
Load Regulation	V_{IN} = 7.0 V	0.15	%
Transient Response	–	3.0	%
Transient Response Time	Load toggle between 0.1 A and 1.0 A	10	μs
Startup Time	–	5.0	ms
Input Voltage			
Start Threshold	–	3.3	V
Sync and Shutdown			
Sync Frequency	–	190 to 355	kHz
Minimum Sync Threshold Voltage	–	1.0	V
Minimum Shutdown Threshold Voltage	–	0.3	V
Maximum Shutdown Bias Current	–	12	μA
General			
Switching Frequency	–	170	kHz
Efficiency	I_{LOAD} = 100 mA I_{LOAD} = 1.0 A	77.5 83	% %
Shutdown Current*	–	1.0	μA

*If a pull−up resistor is employed, the shutdown current is increased drastically (Vin/R).

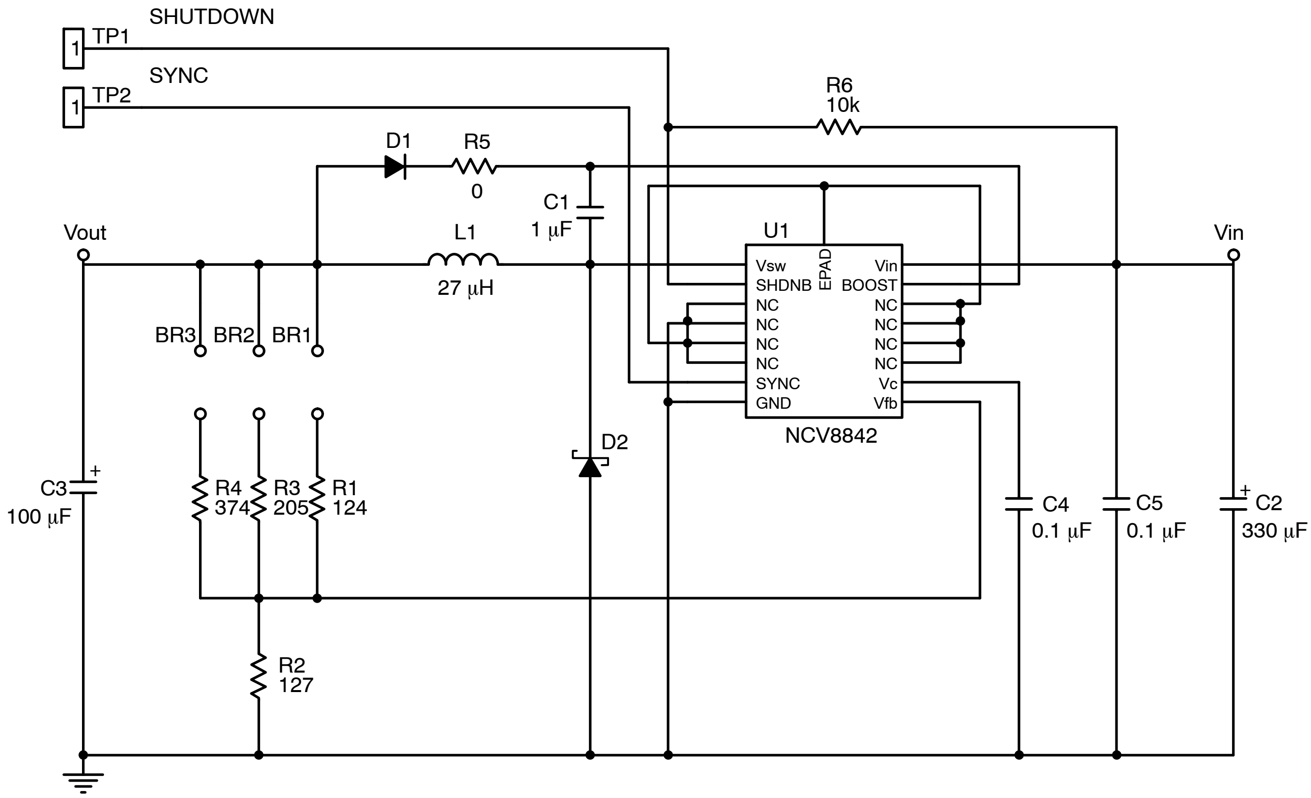


Figure 2. Application Diagram

Operation Guidelines

1. Connect a DC input voltage, within the range of 7.0 V to 16 V, between the board terminals "V_{IN}" (+) and "GND" (−).
2. Connect a load impedance between terminals "V_{OUT}" (+) and "GND" (−).
3. To force the regulator into Shutdown/sleep mode, connect the "SHDNB" terminal to a positive DC voltage of 0.3 V or less, or connect it directly to GND.
4. If synchronization to an external frequency source is desired, connect the SYNC terminal to a pulse source with positive amplitude 1 V to 7 V relative to GND. Sync pulse duty cycle may vary from 10% to 90%.

Theory Of Operation

1. **Boost Circuit:** The Boost circuit, comprised of D1 and C1, generates a voltage higher than the output voltage to drive the base of the internal NPN power switch. When the internal power switch is Off, pin Vsw of the NCV8842 goes negative to sustain the current in L1 through Schottky diode D2. Diode D1 is forward biased, and charges C1 to approximately the output voltage. When the internal power switch turns on, Vsw is driven high, forcing the voltage at BOOST to be the sum of the instantaneous voltage at Vsw plus the charge across C1. D1 is now reverse−biased, and the energy stored in C1 is used to bias the output stage.
2. **Soft Start:** The soft−start is implemented on the V_C pin. During the startup, the limited source current (25 µA) of the error amplifier charges the V_C pin capacitor. The rising slope of the V_C pin voltage clamps the duty cycle through the PWM comparator. The V_C pin voltage eventually settles down to a voltage roughly equal to the reference voltage 1.27 V. Therefore, the startup time can be easily calculated.
3. **Feedback Network:** V^2 control relies on the output ripple to provide pulse width modulation. When the output ripple is inadequate, pulse skipping or instability may be observed. Adding a capacitor C6 in parallel with R1 provides a low impedance pass for the output ripple. Therefore, the output ripple is not attenuated by the resistor divider. The use of this capacitor is optional.

Please see data sheet for more description on regulator operation and component selection (document number NCV8842/D available through the Literature Distribution Center or via our website at http://www.onsemi.com).

TYPICAL PERFORMANCE CHARACTERISTICS

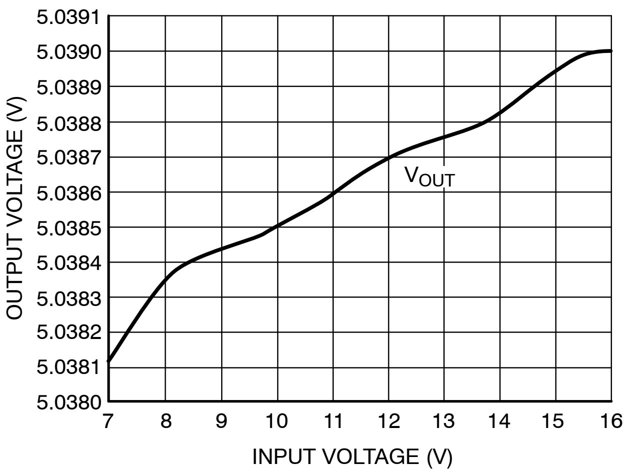


Figure 3. Line Regulation

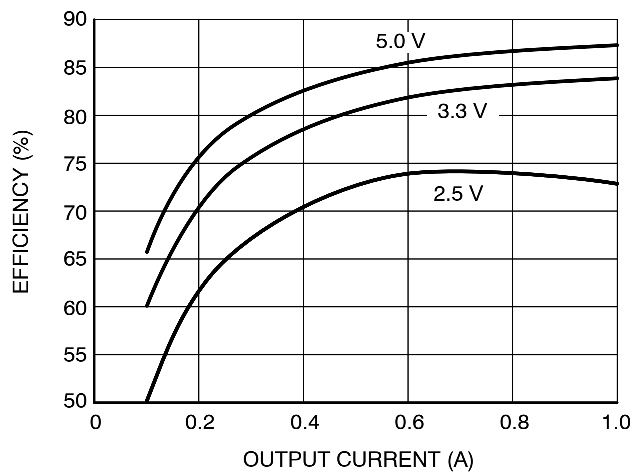


Figure 4. Efficiency vs. Output Current

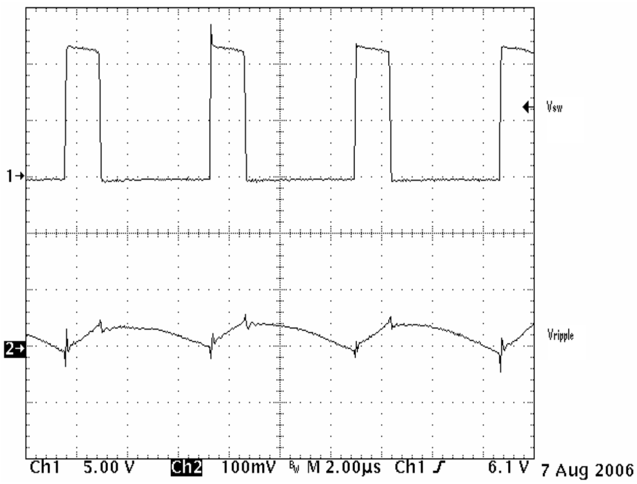


Figure 5. Continuous Mode Operation

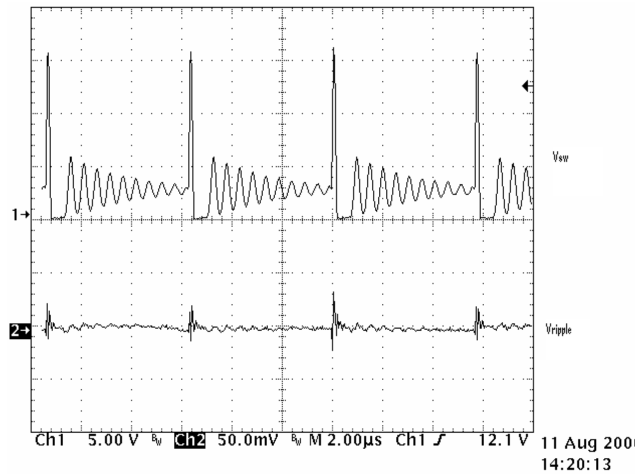


Figure 6. Discontinuous Mode Operation

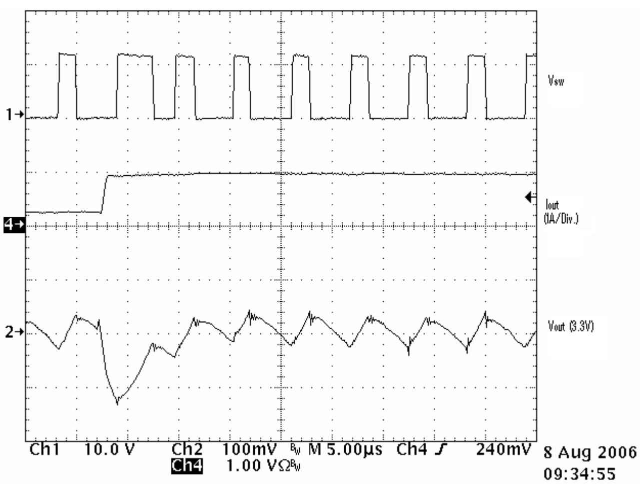


Figure 7. 300 mA to 1.0 A Load Step (3.3 V)

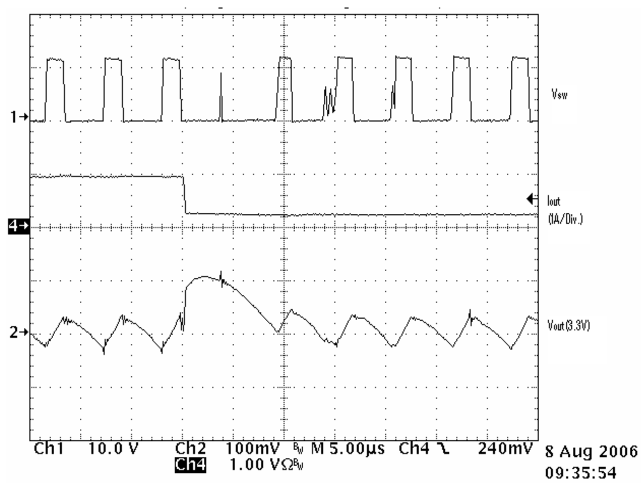


Figure 8. 1.0 A to 300 mA Load Release (3.3 V)

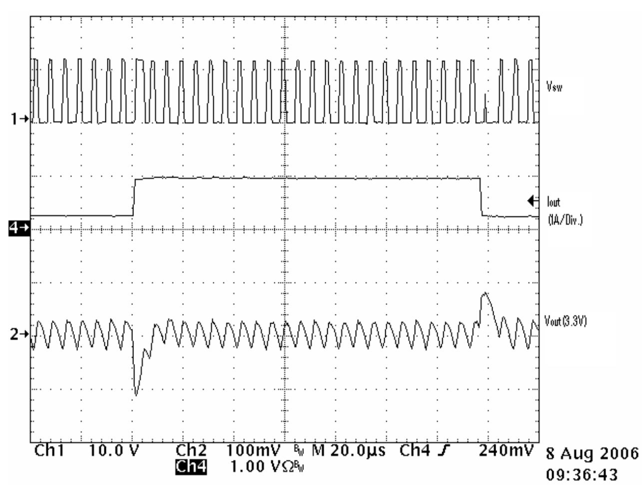


Figure 9. Overall 600 mA Load Response

Table 4. BILL OF MATERIALS

Ref. Designator	Vendor	Part Number	Type	PC/Board
C1	Panasonic	ECJ−1VB0J105K	1 μF Ceramic	1
C2	Panasonic	EEVEC1V331P	330 μF Electrolytic	1
C3	AVX	TAJE107K016R	100 μF Tantalum	1
C4, C5	Panasonic	ECJ−1VBIC104K	0.1 μF Ceramic	2
D1	ON Semiconductor	MBRM130LT3	Diode (Fast Switching)	1
D2	ON Semiconductor	MBRS240T3	2A Diode (Schottky)	1
R1	Panasonic	ERJ−3EKF2040V	124 Ω Resistor	1
R2	Panasonic	ERJ−3EKF1270V	127 Ω Resistor	1
R3	Panasonic	ERJ−3EKF205V	205 Ω Resistor	1
R4	Panasonic	ERJ−3EKF3740V	374 Ω Resistor	1
R5	Panasonic	ERJ−2GEY100V	10 Ω Resistor	1
R6	Panasonic	ERJ−2GEY103V	10 kΩ Resistor	1
L1	Wurth	744771127	27 μH Inductor	1
U1	ON Semiconductor	NCV8842	Controller	1
J1−J8	Vector	K24C/M	Test Points	8
BR1, 2, 3	Molex/Moldom	22−28−4020	Jumpers	3

DRAWINGS OF LAYERS

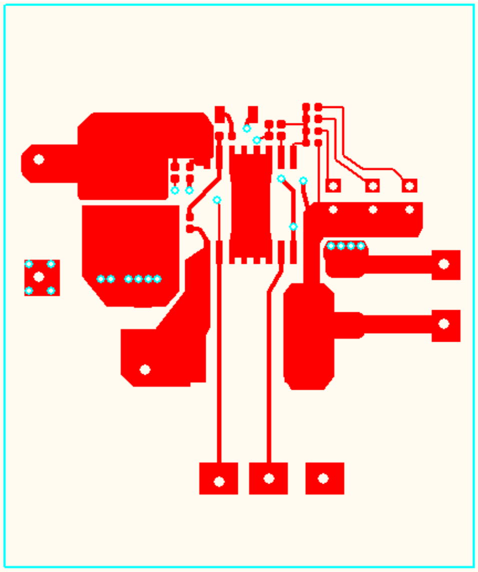


Figure 10. Top Copper

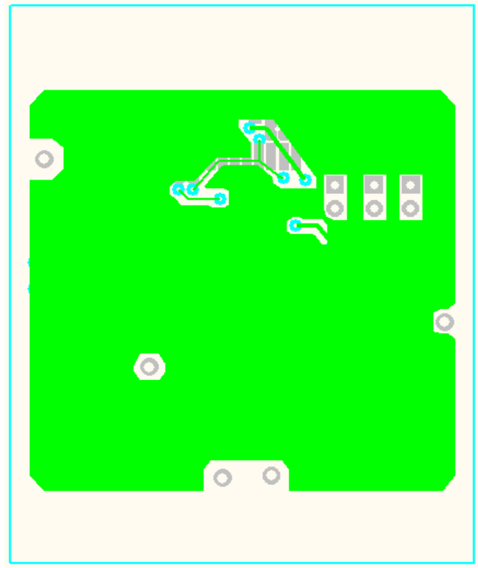


Figure 11. Bottom Copper

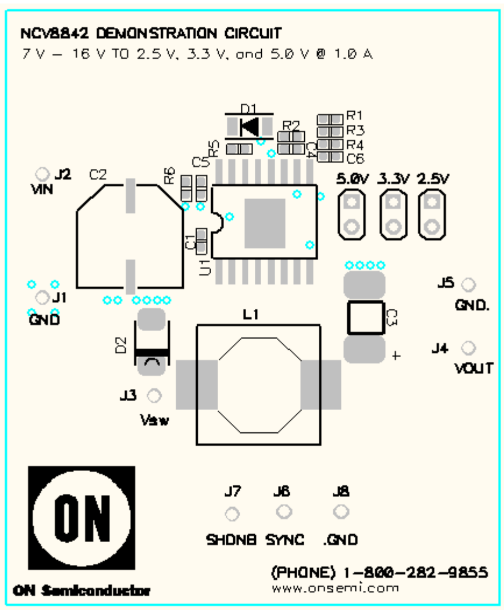


Figure 12. Top Silk

DFN EVALUATION CIRCUIT INFORMATION

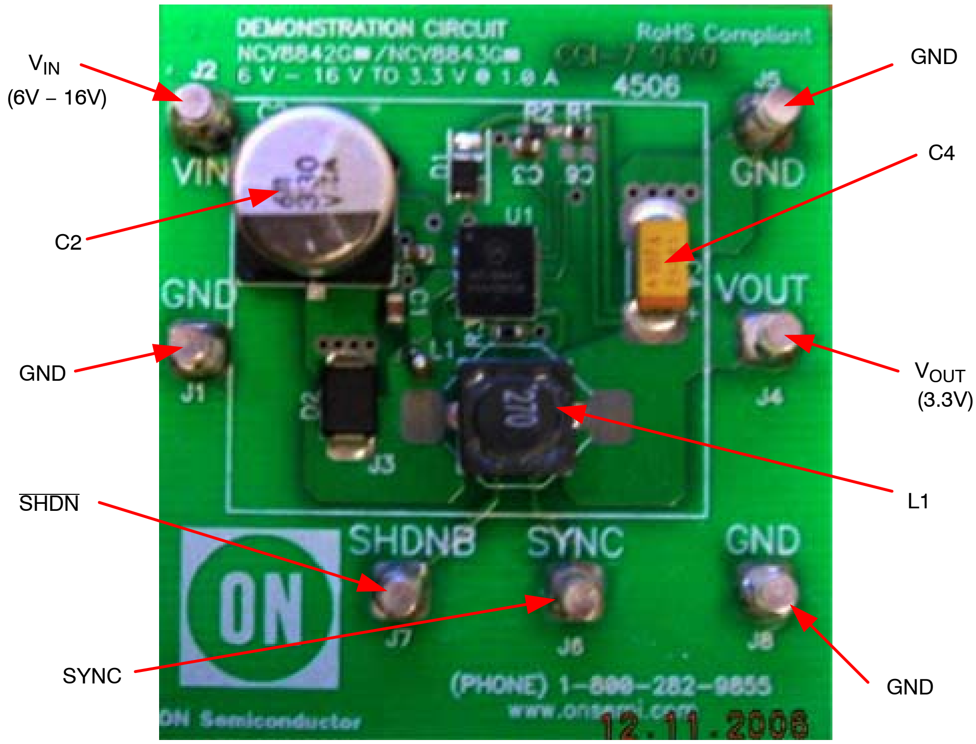


Figure 13. NCV8842 Evaluation Board (DFN Package)

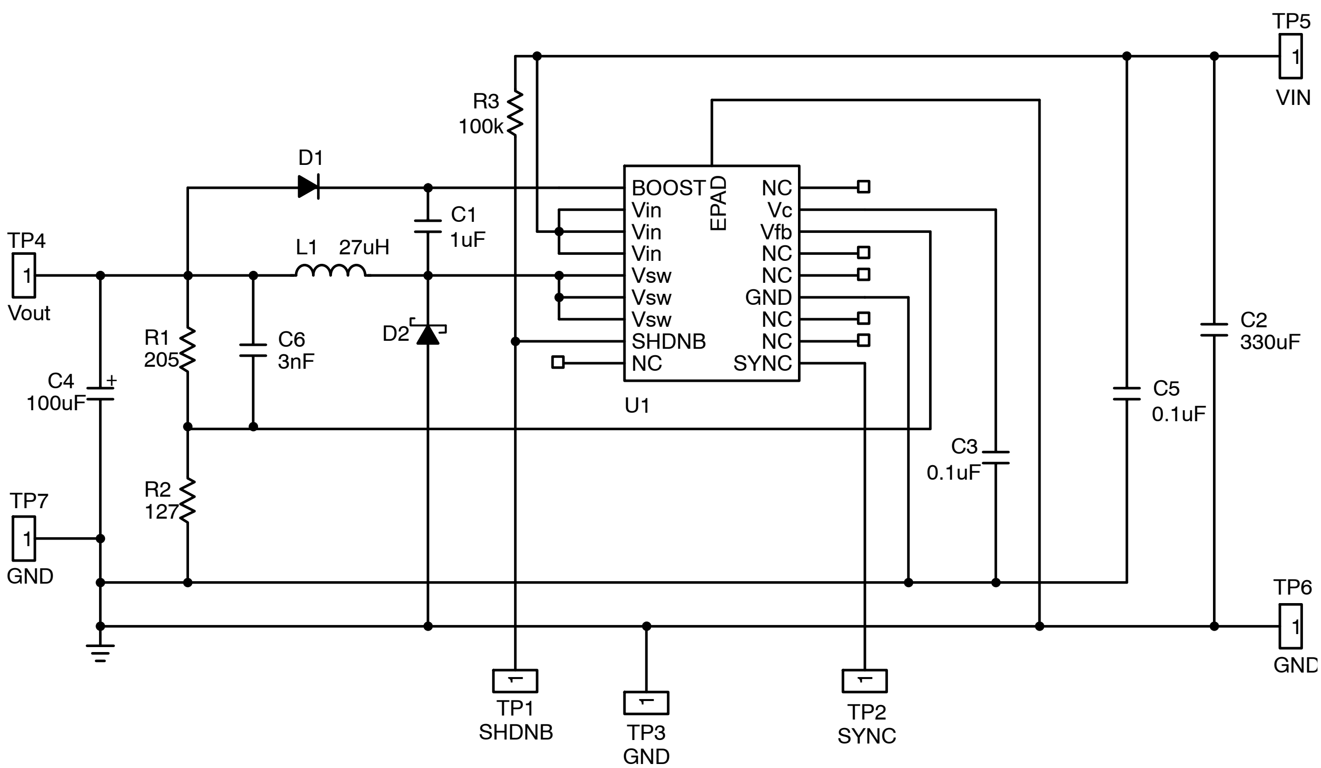


Figure 14. Application Diagram

Table 5. BILL OF MATERIALS

Ref Des	Type	Part Number	Vender	PC/Board
C3, C5	0.1 μF Ceramic	PCC2398CT−ND	Panasonic	2
C1	1.0 μF Ceramic	ECJ−1VBOJ105K	Panasonic	1
C2	330 μF Electrolytic	MZA35VC331MJ10TP	United Chemi−Con	1
C4	100 μF Tantalum	TPSC107K010R0075	AVX	1
C6	3.0 nF Ceramic	Not Used		1
D1	Diode	MBRM130LT1G	ON Semiconductor	1
D2	2 A Schottky Diode	MBRS240LT3G	ON Semiconductor	1
L1	27 μH	7447779127	Wurth	1
R1	205 Ω Resistor	P205HCT−ND	Panasonic	1
R2	127 Ω Resistor	P127HCT−ND	Panasonic	1
R3	100 kΩ Resistor	P100kHCT−ND	Panasonic	1
J1, J2, J4−J8	Test Points	2501−2−00−44−00−00−07−0	Mill−Max MFG	7
J3	Test Point (Vsw)	K24C/M	Vector	1
U1	Regulator	NCV8842G	ON Semiconductor	1

DRAWING OF LAYERS (DFN)

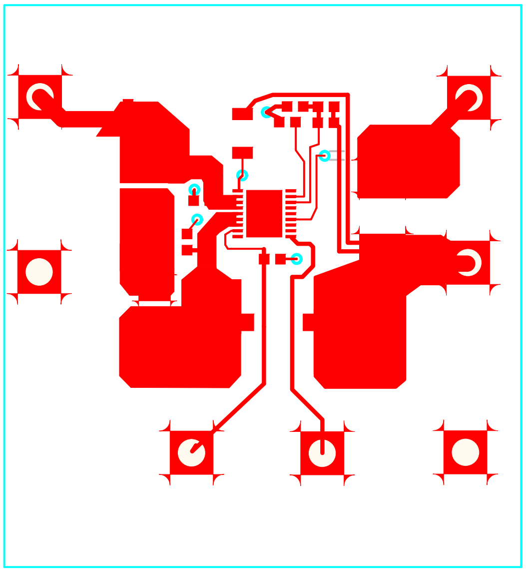


Figure 15. Top Copper

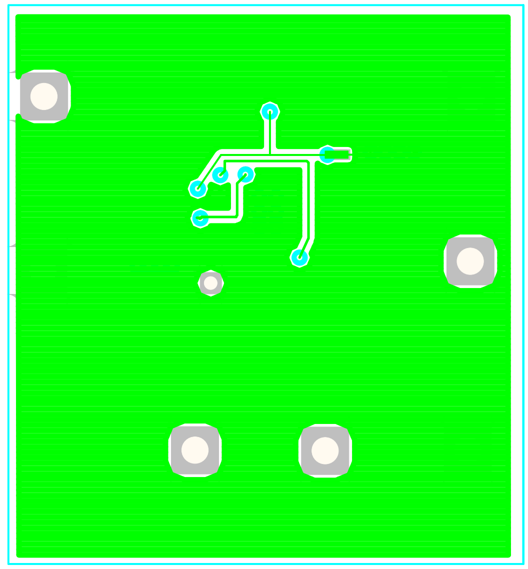


Figure 16. Bottom Copper

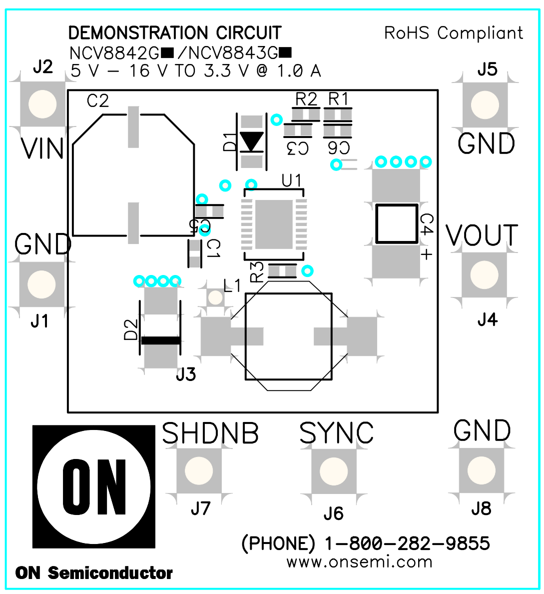


Figure 17. Top Silk

V^2 is a trademark of Switch Power, Inc.

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